CASCADE-ENCODER TECHNIQUE FOR HIGH SPEED ANALOG-TO-DIGITAL CONVERSION

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Abstract

A simple circuit based on a fast operational amplifier, a comparator and a few additional components is used as the basic building block for a high speed analog-to-digital converter of the cascade-encoder type. The properties of this circuit and the performance of an implementation using standard components are discussed. Its potential for LSI is considered.

1. Introduction

The interest in very high speed analog-to-digital converters (ADC's) for digital television, transient recorders and high energy physics instrumentation has led to recent developments in the area of flash ADC's [1-3] using full flash and two step flash techniques. These converters have a typical resolution of 8 bits and a sampling rate of 20 MHz. However, as they require a resistor and a comparator for each channel their complexity increases with 2^n, where n is the number of bits. The large number of comparators being driven in parallel leads to a high input capacitance (in the range 30-300 pF) which requires suitable driving circuits. Also as each comparator is being driven it consumes current and ringing occurs [2]. Thermal effects are still a problem due to the high power dissipated by these devices. Nevertheless flash ADC's seem to be the only practical choice available for very high speed conversion.

Successive approximation converters require a stable input during the full analog-to-digital conversion cycle and therefore are slower than flash ADC's.

Converters of the cascade-encoder type [4, 5], while intrinsically fast and with a complexity that increases only linearly with the number n of bits have not yet been fully exploited.

The circuit we describe in the present work is of the cascade-encoder type and was developed with the aim of finding techniques that could lend themselves to integration with a degree of complexity smaller than that of the flash ADC's.

2. The Basic Module

The cascade-encoder type of ADC here described is based on a circuit module [6] which is shown in Fig. 1. The comparator C is such that for input voltages, V_i, larger than $E_0/2$, where E_0 is the converter input range, it saturates giving an output equal to E_0; otherwise its output is grounded. Therefore the operational amplifier output is equal to $2V_i$ if $V_i<E_0/2$ and equal to $2V_i-E_0$ if $V_i>E_0/2$. At the same time a 0 is presented at the logical output of the circuit in the first case and a logical 1 in the second. The logical output is thus equal to the integer part of the input signal referred to a unit range of $E_0/2$, i.e., it gives the most significant bit of V_i. The linear output, V_0, is equal to the fractional part of the input multiplied by 2. If V_0 is fed to the input of a second circuit identical to the one shown in Fig. 1 the second most significant bit of the initial voltage V_i can be obtained at its logical output. Thus by cascading n elementary circuits of this type an n bit ADC can be obtained as shown in Fig. 2. If a suitable digital delay is used at the logical output of each elementary circuit all the bits corresponding to a same input signal can be made to arrive at the different logical outputs at the same time. Then the conversion rate will depend only on the processing time of just one circuit and, therefore, will not depend on the number of bits being converted.

The behaviour of the basic circuit of Fig. 1 for inputs V_i near the $E_0/2$ threshold was not discussed. For these cases the comparator works in the non saturated region giving an output somewhere between 0 and E_0 which leads to a wrong output, V_0, for the circuit. This difficulty can be easily solved if positive feedback with very little backlash is used in the comparator, i.e., smaller than 1/2 least significant bit.

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3. Experimental Results and Discussion

An implementation of the basic module of Fig. 1 for a voltage range of 0 to 5 V is shown in Fig. 3 and was built on a breadboard. The output of the LM360 comparator with positive feedback is fed to a 4049 CMOS logic inverter to obtain a properly saturated output. An LF357 operational amplifier is used in the output stage. As the open loop gain of the LF357 is reduced to only 20 dB at 1 MHz the measured settling time of the output signal was about 0.5 μs, which corresponds to a sampling rate of 2 MHz. The use of faster amplifiers and a better layout will quite likely improve the speed of the circuit. Actually a straightforward analysis of the circuit of Fig. 1 with an operational amplifier with finite gain A, shows that for an accuracy of 8 bits an open loop gain of 50 to 60 dB is sufficient; lower gain amplifiers are easier to be made fast. The performance of the circuit, even for the case of finite open loop gain, will not be affected by the temperature dependent variation of the two identical resistors R (Fig. 1) since their ratio will remain constant.

The implementation of a 6 bit ADC based in the circuit module of Fig. 3 is shown in Fig. 4. The logic shown has the purpose of introducing successively shorter delays in the logic outputs of the successive circuit modules (1, 2, ..., x, ..., n) so that all the bits corresponding to a same input voltage, V_i, will arrive at the 4035 latch at the same time. This is achieved using one 4015 serial-in/parallel-out shift register per bit, and taking the output from the 4015 pin that has the convenient time delay. This logic assumes that the input is being permanently sampled at the clock rate, once it is initiated by the "start conversion" signal.

The fact that the ADC developed along the concepts here described uses only small to medium scale integrated circuits, is built using repeated modules and has a degree of complexity smaller than that of flash ADC's, seems to indicate that large scale integration or hybrid versions of it can in principle be made.

Acknowledgments

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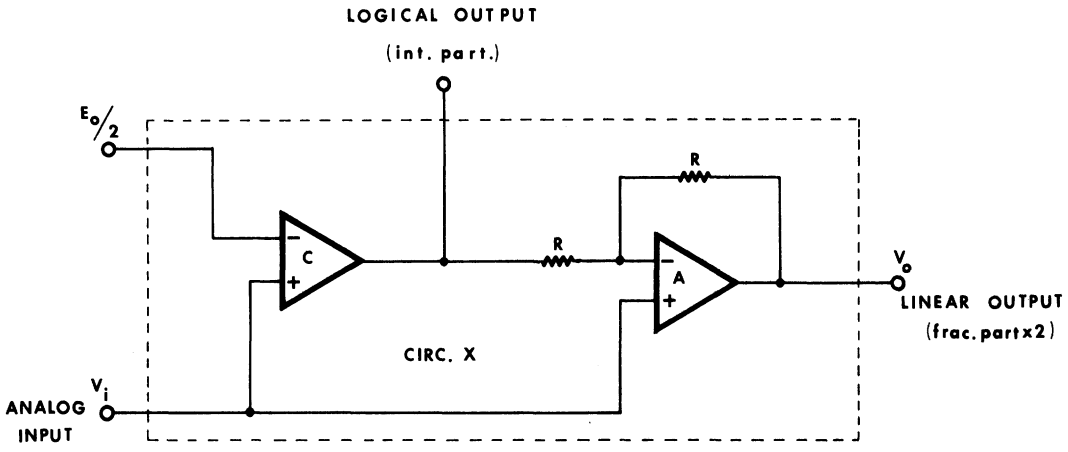

Fig. 1 - Basic Module for Analog-to-digital Conversion.

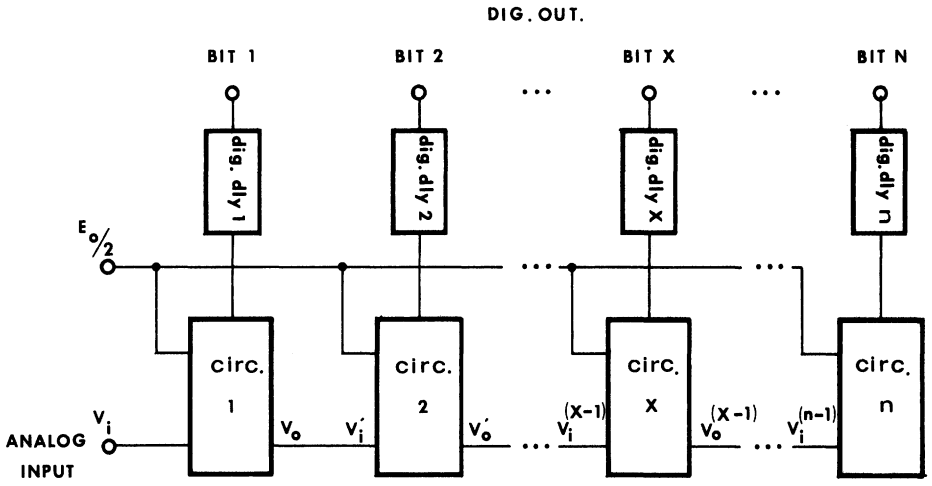

Fig. 2 - Block Diagram of the Analog-to-digital Converter.

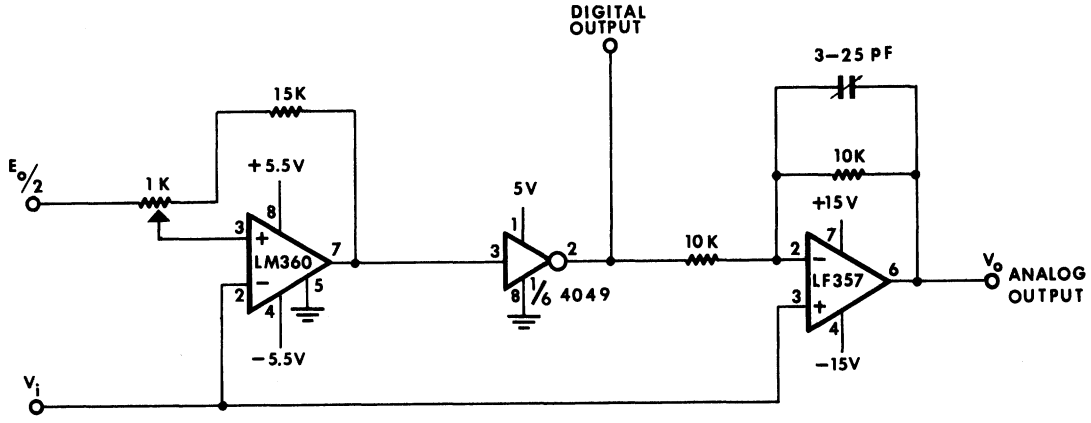

Fig. 3 - Implementation of the Basic Module for Analog-to-digital Conversion.

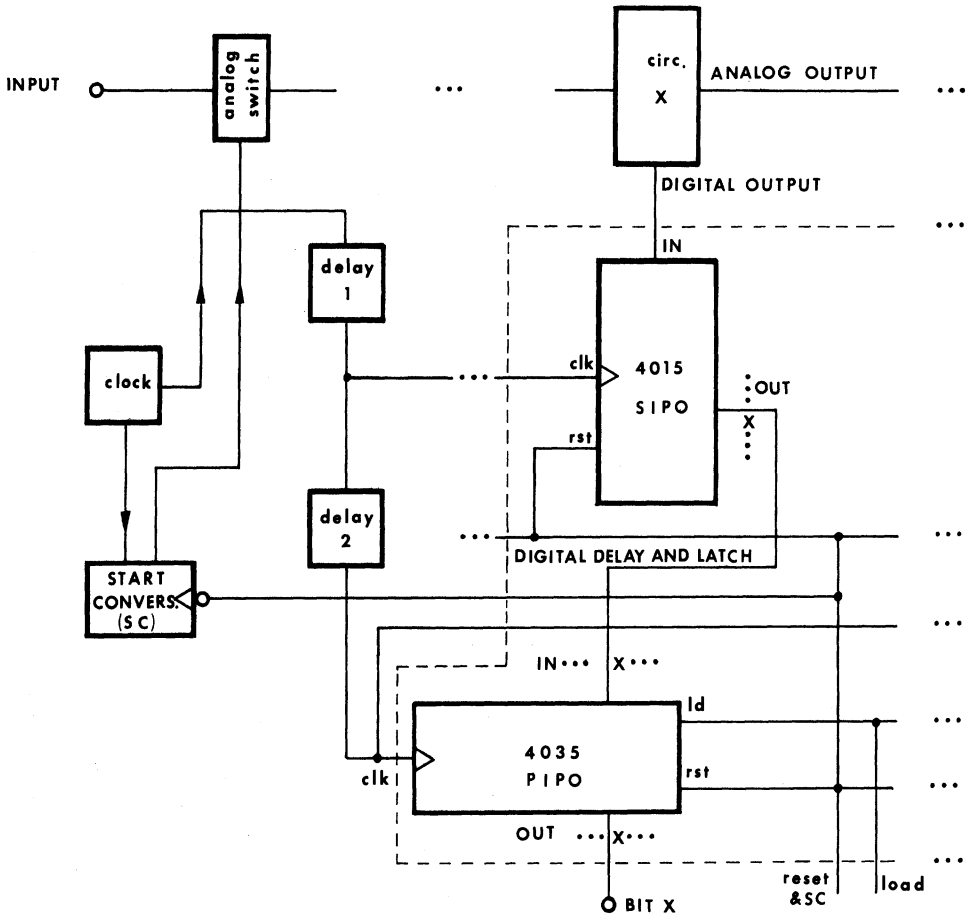

Fig. 4 - Logic for Processing and Control.